



## Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

### Chip to chip interconnect characterization

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#### List of Partners concerned

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<sup>1</sup> **PU** = Public  
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*Deliverable Responsible*

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*Executive Summary*

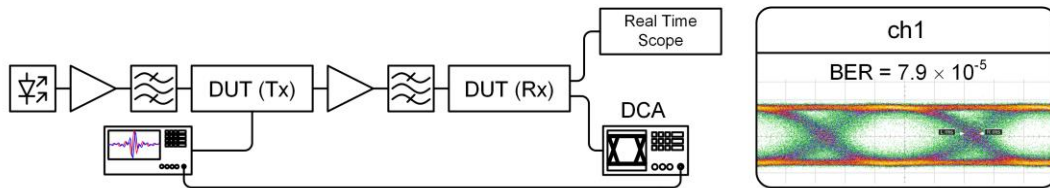
This report contains the testing and evaluation of the chip-to-chip interconnect prototype. In this context, deliverable 6.4 was submitted in accordance with the NAVOLCHI “Description of Work”. The transmitter module consists of a plasmonic modulator and driver array. The receiver is made of Si-Ge photodiodes connected to transimpedance amplifiers. Both modules operated together as a chip-to-chip interconnect in data transmission experiments at 20 Gbit/s.

*Change Records*

Version	Date	Changes	Author
1 (submission)	2015-09-22		Claudia Hoessbacher

## *Plasmonic chip to chip interconnect prototype testing and evaluation*

In a final step, NAVOLCHI's transmitter and receiver (see Milestone42) were tested as a full chip-to-chip interconnect, see Fig. 1. Since time at the end of the project was very limited, only one channel is shown here as an example. The chip-to-chip interconnect successfully operated at 20 Gbit/s with a BER of  $7.9 \times 10^{-5}$ .



**Fig. 1 (a)** Experimental setup for data modulation experiments of the full chip-to-chip interconnect. Laser light at 1547.8 nm was coupled to the transmitter. Electrical data streams were generated by an arbitrary waveform generator (AWG) and sent to the channel under test of the transmitter. The modulated signal was amplified and sent to the receiver. At the receiver output, eye diagrams were measured with a digital communication analyser (DCA), while the bit error ratios were obtained with a real time scope. **(b)** Optical eye diagram of the data experiment (NRZ, rectangular, DBBS 15) at data rates of 20 Gbit/s for Channel 1 as an example.